WE CLAIM:

1. An integrated circuit having copper interconnecting metallization protected by a first overcoat layer, portions of said metallization exposed in a window opened through the thickness of said first overcoat layer, comprising:

   a patterned conductive barrier layer positioned on said exposed portion of said copper metallization and on portions of said first overcoat layer surrounding said window;

   a bondable metal layer positioned on said barrier layer, the thickness of said bondable layer suitable for wire bonding; and

   a second overcoat layer positioned on said first overcoat layer so that the edge of said second overcoat layer overlays the edge of said bondable layer positioned on said portions of said first overcoat layer surrounding said window.

2. The circuit according to Claim 1 wherein said first overcoat thickness is from about 0.6 to 1.5 μm.

3. The circuit according to Claim 1 wherein said first overcoat comprises one or more layers of silicon nitride, silicon oxynitride, silicon dioxide, silicon carbide, or other moisture-retaining compounds.

4. The circuit according to Claim 1 wherein said barrier layer comprises tantalum nitride.

5. The circuit according to Claim 1 wherein said barrier layer is selected from a group consisting of tantalum, titanium, tungsten, molybdenum, chromium, vanadium, alloys thereof, stacks thereof, and chemical compounds thereof.

6. The circuit according to Claim 1 wherein said barrier layer has a thickness between about 0.02 and 0.03 μm.

7. The circuit according to Claim 1 wherein said bondable metal is aluminum or an aluminum alloy.

8. The circuit according to Claim 1 wherein said bondable metal layer has a thickness suitable for wire bonding.

9. The circuit according to Claim 8 wherein said bondable metal layer has a thickness between about 0.4 and 1.4 μm.

10. The circuit according to Claim 1 further comprising a ball bond attached to said plug.

11. The circuit according to Claim 1 wherein said barrier and bondable metal layers overlap between about 0.1 and 0.3 μm over said surrounding portions of said first overcoat layer.

12. The circuit according to Claim 1 wherein said second overcoat comprises one or more layers of silicon nitride, silicon oxynitride, silicon dioxide, silicon carbide, or other moisture-retaining compounds.

13. The circuit according to Claim 1 wherein the thickness of said second overcoat layer is approximately equal to the sum of the thicknesses of said barrier and bondable layers.

14. The circuit according to Claim 1 wherein said second overcoat layer has a thickness between about 0.6 and 2.0 μm.

15. The circuit according to Claim 1 wherein said overlay of said second overcoat over the edge of said bondable layer is between about 0.1 and 0.3 μm.

16. A wafer-level method of fabricating a metal structure for a contact pad of an integrated circuit having copper interconnecting metallization protected by a

first overcoat layer including insulating silicon compounds, a window opened through the thickness of said first overcoat layer to expose portions of said copper metallization, the method comprising the steps of:

depositing a barrier metal layer over said wafer to cover said exposed copper metallization and first overcoat surface;

depositing a bondable metal layer over said barrier layer in a thickness sufficient to fill said overcoat window and to enable wire ball bonding;

patterning both said deposited metal layers so that only the layer portions inside the window and over a first overcoat area close to the window perimeter remain;

depositing a second overcoat layer including insulating silicon compounds over said wafer;

patterning said second overcoat layer so that only the layer portions on said first overcoat layer and the edge of said bondable layer surrounding the perimeter of said window remain; and

selectively removing said second overcoat layer from said bondable metal layer to expose said bondable metal for the process of wire bonding.

17. The method according to Claim 16 wherein said step of selectively removing said second overcoat layer comprises photoresist, photomask, and etching techniques.